A DC/AC CONVERTER WITH RESONANT CIRCUIT AT THE INPUT AND INTERMEDIATE RF CIRCUIT

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Abstract

The paper presents a new type of DC/AC converter with resonant circuit at the input and intermediate RF circuit, aimed at feeding a mono-phase consumer from an accumulator battery. In this way, the commutation losses in converter's semiconductor devices are reduced, while the problems of electromagnetic interference become less severe, once the resonant pulses have lower dv/dt slopes.

1. Introduction

During the last years, a considerable research efforts have been performed to elaborate converters with resonant circuits in which the solid state devices switching is performed at zero voltage (ZVS) or zero current (ZCS) [1,2,3].

A DC/AC converter with resonant circuit, operating on this principle has the following advantages [4] :

- the devices switching losses at both turn-on and turn-off vanish giving high converter efficiency;
- the electromagnetic interference (EMI) problem is less severe because the resonant pulses have lower dv/dt compared to those of a hard switched converter,
- the converter can be operated without snubbers;
- the devices heating is low, resulting only from the conduction loss, therefore cooling requirement is low;
- all the above factors make the converter size smaller and also reduce the converter cost.

The purpose of this paper is to propose a new type of DC/AC converter with resonant circuit that is operated when the semiconductor device switchings take place.

2. Operation of the resonant circuit

Figure 1 shows a DC/AC converter with both resonant circuit and intermediate RF circuit.

The converter is composed of an inverter with 4 IGBT devices $T_1 - T_4$, a ferrite transformer and a cycloconverter containing 4 IGBT devices $T_A - T_D$[5,6,7].

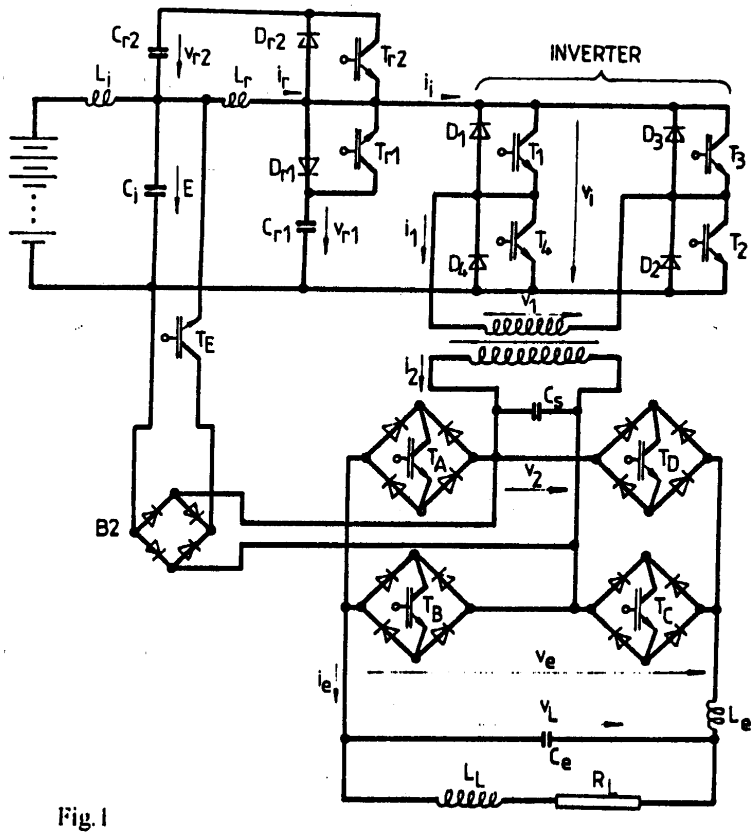


Fig. 1

For the IGBT switchings to be soft, the resonant circuit is operated in order the obtain zero voltage at the inverter input. Before the switching moments, the resonant capacitor C_{r1} and clamp capacitor C_{r2} are charged to the voltages $v_{r1} = K'E$, and respectively $v_{r2} = (K'-1)E$.

K' is the real clamping ratio, having a value between 1.3 and 1.5, higher than the ideal clamping ratio K, that can be chosen using the relation [7,8]:

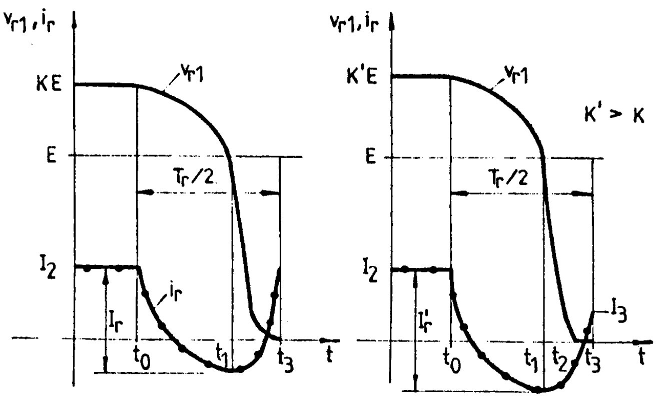
$$K = 1 + \sqrt{\frac{C_{r_1}}{C_{r_1} + C_{r_2}}} \qquad (1)$$

The clamping ratios K and K', can be defined according to fig. 2.

In the case shown in fig.2a, at the moment t_0, when $v_{r1} = KE$, T_{r1} and T_{r2} are turned - on and at the moment t_1, the voltage V_{r1} becomes equal to E while the current through the induction L_r has the value:

$$i_r = I_2 - I_r = I_2 - (K-1)E\sqrt{\frac{C_{r_1} + C_{r_2}}{L_r}} = I_2 - E\sqrt{\frac{C_{r_1}}{C_{r_2}}} \qquad (2)$$

Then at the moment t_1, T_{r2} is turned-off and the voltage v_{r2} remains zero. The capacitor C_{r1} continues discharging until the voltage v_{r1} reaches zero, at the moment t_3.



a. b.

Fig.2

At this last moment, the current i_r becomes equal to the load current I_2.
The duration of the resonant process T_r is given by the relation :

$$T_r = 2\pi \sqrt{L_r(C_{r_1} + C_{r_2})} + 2\pi\sqrt{L_r C_{r_1}} = 2\pi\sqrt{L_r C_{r_1}} \cdot \frac{K}{K-1} \qquad (3)$$

In the case shown in fig. 2b ,at the moment t_0,when v_{r1} $K'E$ (K'>K),the transistors T_{r1} and T_{r2} are turned -on and the voltage v_{r1} equals E at the moment t_1, but the maximum value of the resonant current is given by the relation:

$$I'_r = (K'-1)E\sqrt{\frac{C_{r_1} + C_{r_2}}{L_r}} = \frac{K'-1}{K-1} E \sqrt{\frac{C_{r_1}}{L_r}} > I_r \qquad (4)$$

At the moment t_1, T_{r2} is turned-off while the capacitor C_{r1} continues to discharge until the voltage v_{r1} reaches zero, at the moment t_2 .Between t_2 and t_3 the voltage v_{r1} is maintained zero due to to the inverter diodes. Finally, at the moment t_3, the current i_r reaches a value I_3 lower than I_2.

In both cases shown in fig.2a and b, it was considered that one switching of the inverter transistors takes place at the moment t_3.

Forward, the operating mode of the converter shown in fig.1 is described during a switching process, for example, the one starting at the moment t_0 according to figs. 1 and 3.
At the moment t_0, the transistors T_1 and T_2 are on, the voltage on the primary winding of the RF transformer is equal to $K'E$ and the input inverter current i_i equals I_d.

At the moment t_0, the transistors T_{r1} and T_{r2} are turned-on, so between t_0 and t_1 the voltages v_{r2} and v_{r1} decrease from $(K'-1)E$ to zero and respectivelly, from $K'E$ to E (figs. [illegible] and c).

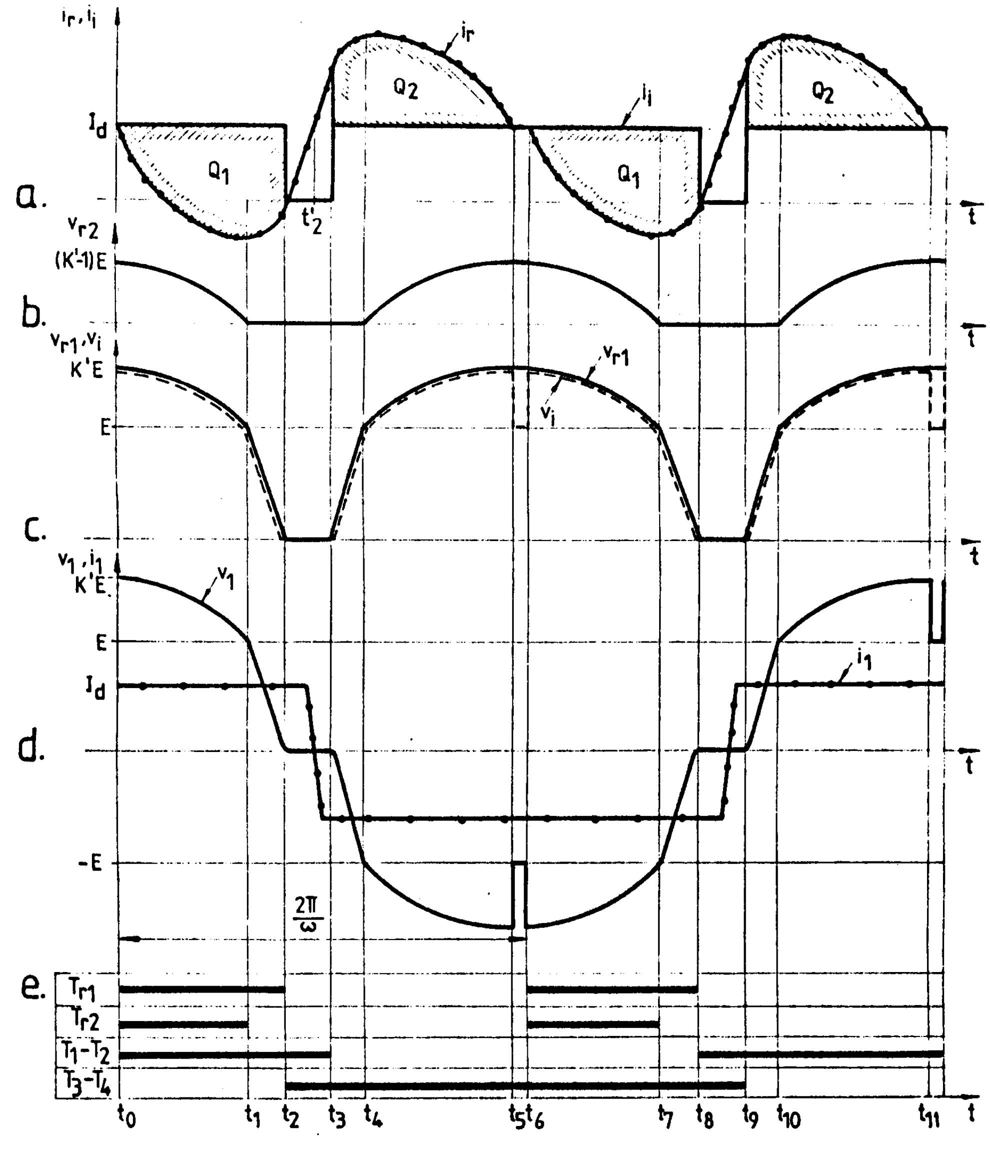


Fig.3

At the moment t_1, the current i_r through the inductor L_r reaches the value $(I_d-I'_r)$. Then, only the capacitor C_{r1} continues to discharge through T_{r1} until it reaches zero voltage at the moment t_2, since T_{r2} is turned-off at the moment t_1.

The voltage v_{r1} remains zero up to the moment t_3, when the transistors T_{r1}, T_1, T_2 are turned-off and the devices T_3 and T_4 are turned-on. Obviously, the moment t_3 is imposed by the converter command pattern.

At the moment t_3, the current i_i reaches a value I_d (fig.3a).

Then, up to the moment t_4, capacitor C_{r1} charges from zero to the voltage value E through the diode D_{r1} and between t_4 and t_5, C_{r1} and C_{r2} overcharged up to $K'E$ and respectively $(K'-1)E$. Between t_5 and t_6, the voltage $v_i = E$ is applied to the inverter's input. During the interval time, the current i_r becomes again equal to the inverter current $i_i = I_d$. At the end of this interval time, a new operating cycle of DC/AC converter begins. On the constant operating regime of the converter the hachured areas in fig.3a, which represent: Q_1 - the electric charge lost by the capacitors and Q_2 - the electric charge received by the capacitors, become equal (thus $Q_1 = Q_2$).

Finally, in what follows, the waveforms of the output voltage v_2 on the terminals of the secondary winding of the transformer is explaind, according to fig.4.

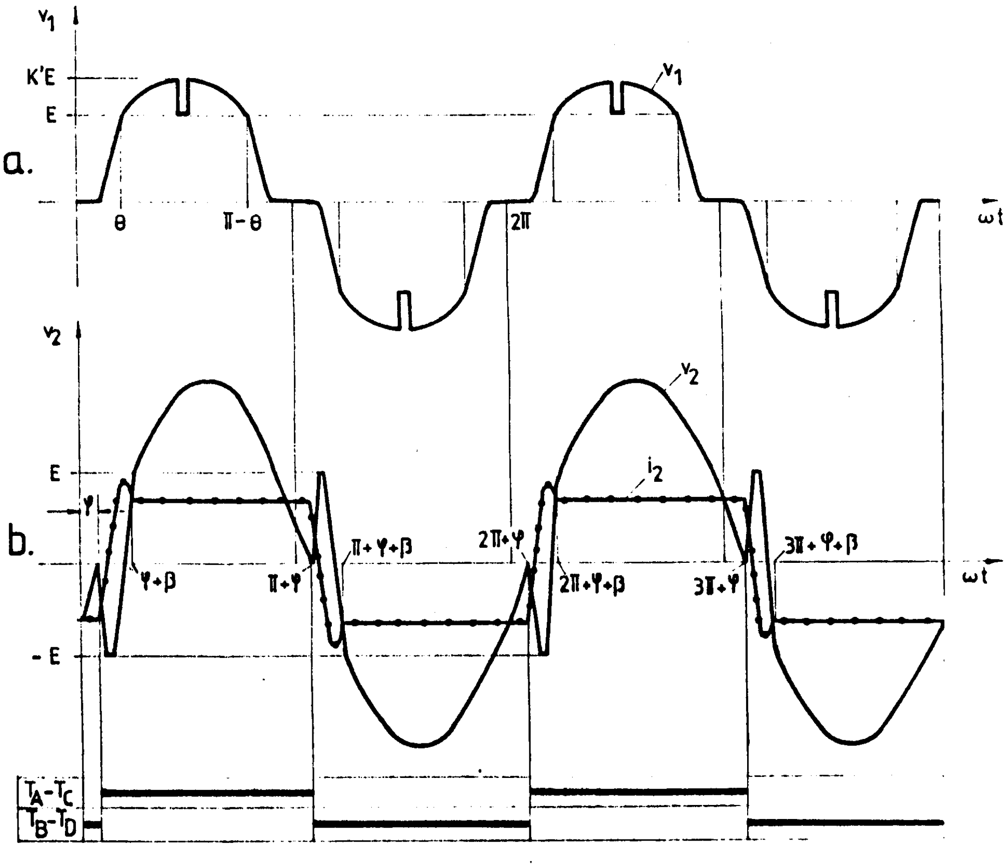


Fig.4

Fig.4a shows the voltage v_1 for two periods and fig.4b shows the voltage v_2 and the current i_2. The φ angle represents the phase difference between the fundamentals $V_{1(1)}$ and $V_{2(1)}$ of the two voltages. Along the two periods, the value of the load current i_2 is considered as remaining constant. The switchings of the transistors T_A -T_D occur at φ, $\pi+\varphi$, $2\pi+\varphi$, $3\pi+\varphi$ angles and so on, when the voltage v_2 is canceled.

Simultaneously with these switchings , the transistor T_E is turned-on at ZCS. After performing these switchings, the difference current (i_e-i_2) charges the switching capacitor C_s up to the voltage E. The diode bridge opens and the excess of inductive energy flows into the capacitor C_1 through the transistor T_E. The necessary switching angle for the current i_2 to change direction is β and it is shown in fig.4b.

Its value is chosen so that dv_2/dt of the voltage on the secondary winding should be acceptable for the semiconductor devices. At the end of the switching angleβ, the ZVS of the transistor T_E takes place.

3. DC/AC Converter with one PWM Based Inverter

The operating principle of DC/AC converter with one PWM inverter and one RF intermediate circuit results from fig.5a. By means of the cycloconverter having the T_A - T_D transistors, on the load pulse trains are applied consisting of the integers p_1, p_2, ...,p_6 of pulses.

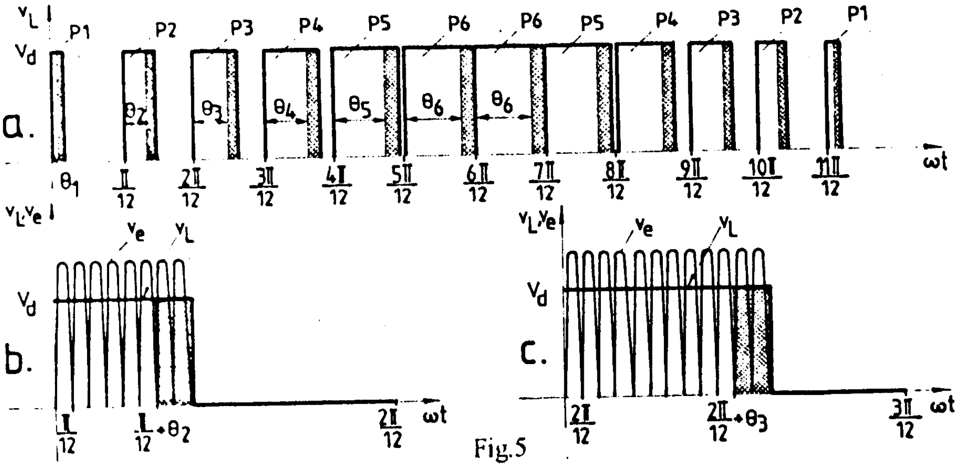


Fig.5

These pulse trains are pulse width modulated according to a sinusoidal law so that the low order (n = 3,5,7,etc) higher harmonics of the output voltage v_e of the cycloconverter have small values, generally less than 5% of the value of the fundamental amplitude $V_{e(1)}$.

For an output frequency f =50Hz of the fundamental voltage $v_e(1)= V_e(1) \sin(2\pi f t)$ the pulse frequency f_p is adopted as 24 Khz. Since the voltage E of the accumulator battery can decrease with about 20% from its maximum value E_{max}, in order to keep the fundamental amplitude $V_{e(1)}$ practically unchanged, certain modes of operation (for example A,B,...,E are chosen, differing from each other by the number of pulses obtained at the cycloconverter output.

For instance, fig.5b shows the fact that within the interval $\pi/12$ and $2\pi/12$, the pulse number can change between $p_2 = 6$ (for E_{max}) and $p_2 = 8$ (for $0,8\ E_{max}$).

At the same time, fig.5c presents the variation of the pulse number p_3 within the interval $2\pi/12$ and $3\pi/12$.

The values of the pulse numbers on different intervals of the fundamental period are given in Table 1 depending on the chosen operation mode:

Table 1

OPERATION MODE	PULSE NUMBER p_1	p_2	p_3	p_4	p_5	p_6	VOLTAGE E
A	3	8	12	16	19	20	80,19%Emax
B	3	8	12	15	18	19	86,16%Emax
C	3	7	11	15	17	18	90,81%Emax
D	2	7	11	14	16	17	95,61%Emax
E	2	6	10	13	15	16	100%Emax

During the pauses when the voltage v_e vanishes (Fig.5a), the current i_e closes through the transistors T_A and T_D or T_B and T_C. Obviously, for the sake of simplicity in the control diagram of the DC/AC converter, only two of the cycloconverter's transistors are in conduction during one pause.

The two groups of transistors are in conduction alternatively, during two joining pause intervals.

Certainly, during the pause intervals the resonant circuit and the inverter are not working, the transistors T_{r1}, T_{r2} and T_1 - T_4 being turned - off.

At the beginning of a pause interval, the secondary winding of the ferrite transformer is still connected only with the switching capacitor C_s whose voltage increases with the permitted slope dv_2/dt up to the value E. Since the primary winding is connected to the capacitor C_{r1} having a reduced voltage $v_{r1} < E$ (fig.4a), part of the energy stored by C_s will be transfered to the capacitor C_{r1} by means of the diodes D_1 -D_4 and D_{r1}.
This energy transfer results in the increase of the DC/AC converter efficiency.

The higher harmonis in the spectrum of the output voltage v_e are those of the order (f_p /f - 1) and (f_p /f +1). These harmonics can be considerably decreased by introducing the passive filter L_e - C_e at the cycloconverter output.

In fig.6 are presented the ratios between the amplitudes $V_{(n)}$ of the main higher harmonics of the voltage applied across the load, and the amplitude $V_{(1)}$ of the fundamental corresponding to the A operation mode. One can draw the conclusion that, regarding the higher harmonics of the current passing through the load, their amplitude are smaller than 5% from the condition that the power factor of the load is inductive and less than about 0.9

As a conclusion, the DC/AC converter proposed in fig.1 is adequate for its [illegible] at relatively small output ranging between hundreds of W and some KW, only one ferrite transformer being enough in this case. What concerns the load impedance, its inductive power factor must be smaller than 0.9.

Certainly, in the case of an output frequency f = 60 Hz, other operation modes can be conceived, characterized by different pulses numbers.

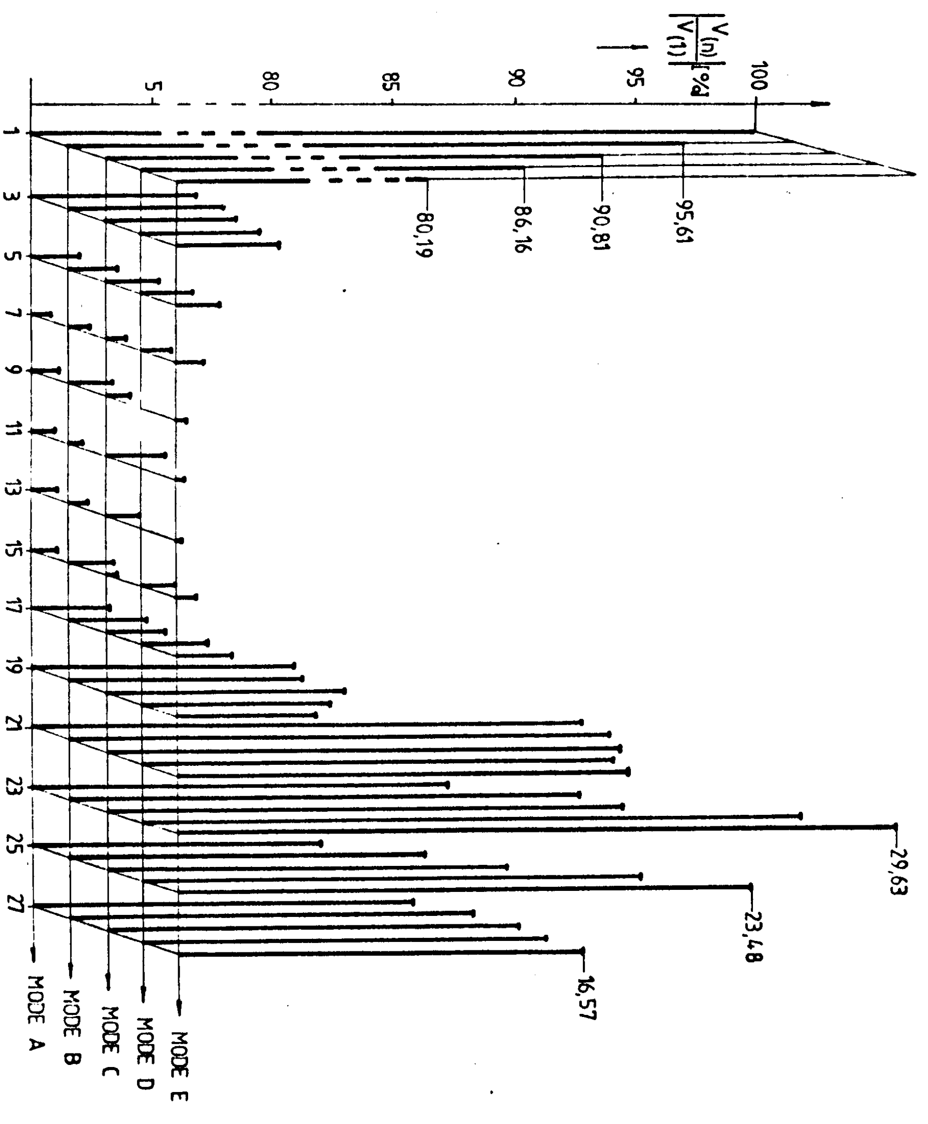

|V(n)| / |V(1)| [%]
100
95
90
85
80
5
95,61
90,81
86,16
80,19
29,63
23,48
16,57
1
3
5
7
9
11
13
15
17
19
21
23
25
27
MODE A
MODE B
MODE C
MODE D
MODE E

Fig.6

4. DC/AC Converter with More Inverters with Asymmetric Control

Figure 7 presents the basic diagram of the DC/AC converter with an input resonant circuit, three inverters, tree ferrite transformers and one cycloconverter having the [illegible] transistors.

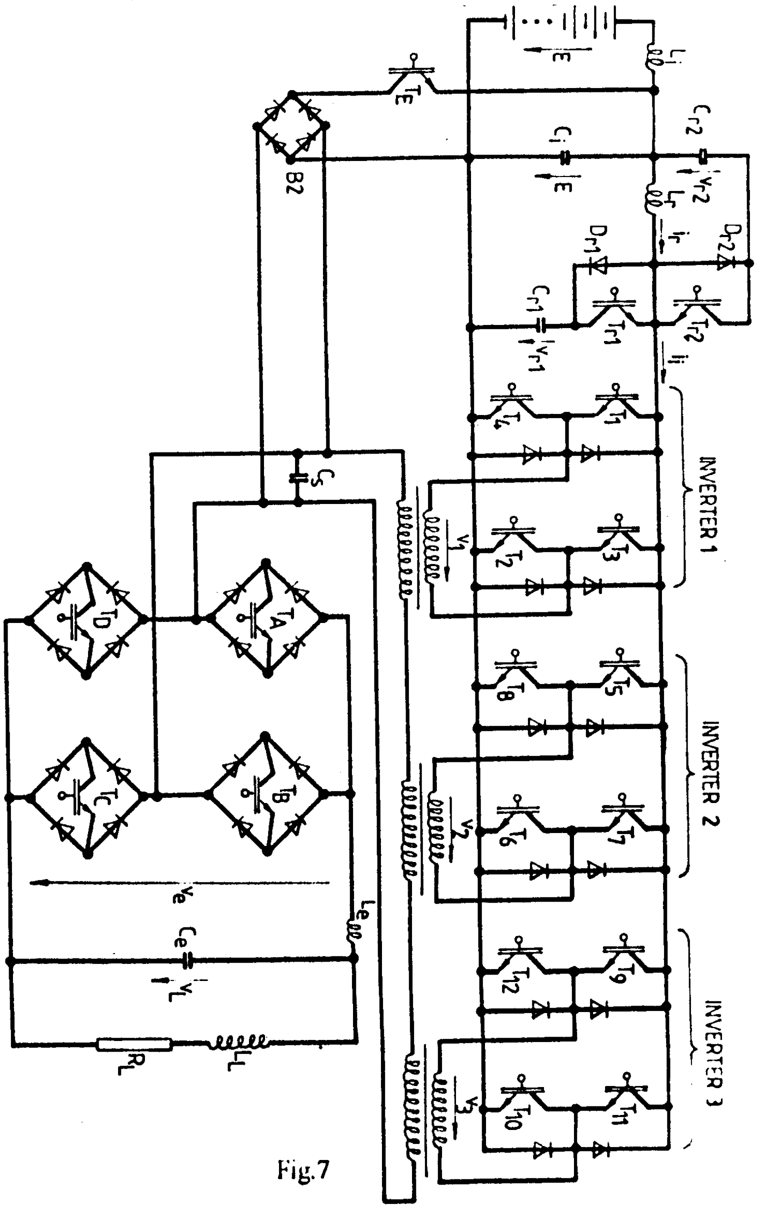


Fig.7

The operating principle of this DC/AC converter results from fig.8.

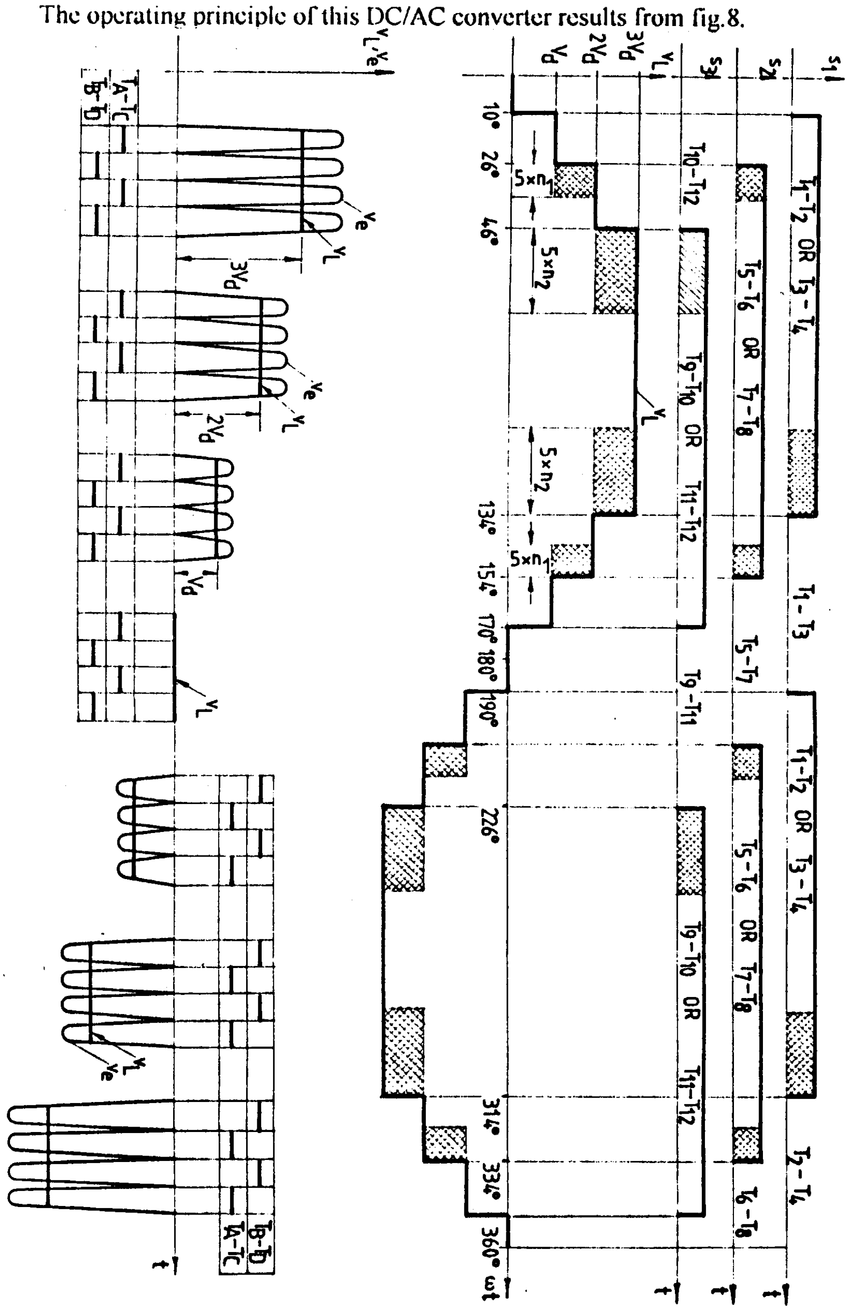


Fig.8

Here the signals S_1, S_2 and S_3 show the working durations of the three inverters with asymmetric control.

The waveforms of the voltages v_1, v_2 and v_3 applied at the primary windings of the ferrite transformers are identical with those presented in fig.4.

The voltage pulses obtained at the transformers output windings are summed and by means of the T_1 - T_6 transistors of the cycloconverter, the load voltage v_L presented in fig.8 is obtained. The pulse frequency f_p can be chosen 18 Khz (for f = 50 Hz) or 21,6 Khz (for f = 60 Hz).

These values were obtained considering that 360 pulses correspond to one fundamental period.

For this DC/AC converter more operation modes (A, B, C,..., F) are also established, so that, when the voltage of the accumulator battery changes between 82,2% and 100% from the value E_{max}, the output voltage applied across the load remains practically unchanged.

These working modes can be obtained by eliminating, step by step , a number of pulses equal to $n_1 = 2$ and $n_2 = 5$, from the hachured surfaces in fig.8.

Table 2 presents, for a half-period, the limit values, given in grades, of the inverters working durations S_1, S_2 and S_3 for different working modes (A, B, C,..., F).

Table 2

Working mode	S_1	S_2	S_3	Voltage E
A	10 ° – 134 °	26 ° - 154 °	46 ° - 170 °	82,20% E_{max}
B	10 ° - 129 °	28 ° - 152 °	51 ° - 170 °	86,13% E_{max}
C	10 ° - 124 °	30 °- 150 °	56 ° - 170 °	89,89% E_{max}
D	10 ° - 119 °	32 ° - 148 °	61 ° - 170 °	93,47% E_{max}
E	10 ° - 114 °	34 ° - 146 °	66 ° - 170 °	96,85% E_{max}
F	10 ° - 109 °	36 °- 144 °	71 ° - 170 °	100 % E_{max}

Figure 9 presents the ratios between the amplitudes $V_{(n)}$ of the most important higher harmonics of the voltage across the load, and the fundamental amplitude $V_{(1)}$ corresponding to the A operation mode.

A comparison between the higher harmonics spectrums related to the outout voltages v_L of the DC/AC converters according to figs. 6 and 9, reveals that the version presented in fig.7 is more advantageous, being characterized by a lower content of higher harmonics.

In the case of the DC/AC converter with three ferrite transformers, the higher harmonics of the current passing through the load can have amplitudes lower than 5% of the current fundamental value, under the condition that the load power factor is inductive and smaller than 0,95.

No doubt, DC/AC converters with more than three ferrite transformers can be conceived, and in this case the voltage higher harmonics will reduce even more.

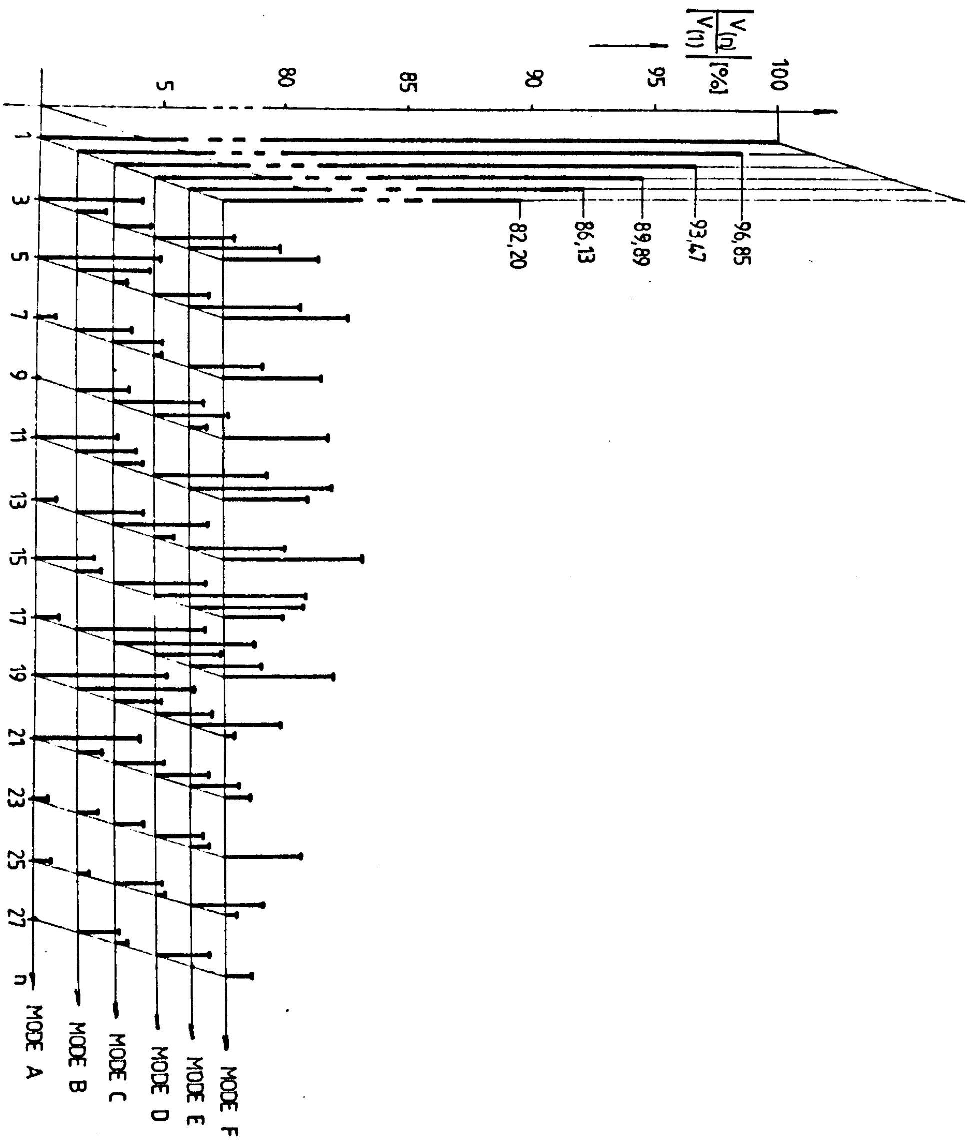


Fig.9

As a conclusion, the DC/AC converter proposed in fig.7 is adequate to be used for relatively high output powers, ranging between some KW and tens of KW.

Based on the diagrams presented in figs. 1 and 7, DC/AC converters can be realised whose output voltage in three - phased [9].

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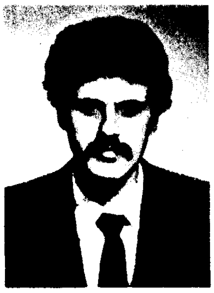

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