A DC/AC CONVERTER WITH RESONANT CIRCUIT AT THE INPUT AND INTERMEDIATE RF CIRCUIT

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Abstract

The paper presents a new type of DC/AC converter with resonant circuit at the input and intermediate RF circuit, aimed at feeding a mono-phase consumer from an accumulator battery. In this way, the commutation losses in converter's semiconductor devices are reduced, while the problems of electromagnetic interference become less severe, once the resonant pulses have lower dv/dt slopes.

1. Introduction

During the last years, a considerable research efforts have been performed to elaborate converters with resonant circuits in which the solid state devices switching is performed at zero voltage (ZVS) or zero current (ZCS) [1,2,3].

A DC/AC converter with resonant circuit, operating on this principle has the following advantages [4]:

- the devices switching losses at both turn-on and turn-off vanish giving high converter efficiency;
- the electromagnetic interference (EMI) problem is less severe because the resonant pulses have lower dv/dt compared to those of a hard switched converter;
- the converter can be operated without snubbers;
- the devices heating is low, resulting only from the conduction loss, therefore cooling requirement is low;
- all the above factors make the converter size smaller and also reduce the converter cost.

The purpose of this paper is to propose a new type of DC/AC converter with resonant circuit that is operated when the semiconductor device switchings take place.

2. Operation of the resonant circuit

Figure 1 shows a DC/AC converter with both resonant circuit and intermediate RF circuit.

The converter is composed of an inverter with 4 IGBT devices $I_{1} \ldots I_{4}$, a ferrite transformer and a cycloconverter containing 4 IGBT devices $I_{5} \ldots I_{8}$ [5,6,7].
Fig. 1

For the IGBT switchings to be soft, the resonant circuit is operated in order to obtain zero voltage at the inverter input. Before the switching moments, the resonant capacitor \( C_1 \) and clamp capacitor \( C_2 \) are charged to the voltages \( v_1 = K'v' \), and respectively \( v_2 = (K'-1)v' \).

\( K' \) is the real clamping ratio, having a value between 1.3 and 1.5, higher than the ideal clamping ratio \( K \), that can be chosen using the relation [7,8]:

\[
K - 1 = \sqrt{\frac{C_n}{C_n + C'_h}}
\]

(1)

The clamping ratios \( K \) and \( K' \) can be defined according to fig. 2.

In the case shown in fig.2a, at the moment \( t_0 \), when \( v_{KL} = v'E \), \( T_{r1} \) and \( T_{r2} \) are turned on and at the moment \( t_1 \), the voltage \( V_{r1} \) becomes equal to \( E \) while the current through the induction \( L_I \) has the value:

\[
ir = i_z - i_z - (K-I)E = \frac{C_n + C'_n}{L_I} = i_z - E \sqrt{\frac{C_n}{C'_n}}
\]

(2)

Then at the moment \( t_1 \), \( T_{r2} \) is turned-off and the voltage \( v_{KL} \) remains zero. The capacitor \( C_{11} \) continues discharging until the voltage \( v_{KL} \) reaches zero, at the moment \( t_s \).
At this last moment, the current \( i_t \) becomes equal to the load current \( I_2 \).

The duration of the resonant process \( T_r \) is given by the relation:

\[
T_r = 2\pi \sqrt{\frac{L_r (C_{n1} + C_{n2})}{L_r C_{n2}}} + 2\pi \sqrt{\frac{L_r C_{n2}}{L_r C_{n1}}} = 2\pi \frac{K}{K' - 1 - 1}
\]  
(3)

In the case shown in fig. 2b, at the moment \( t_0 \) when \( w_{p1} = K'E' \) (K' > K), the transistors \( T_{r1} \) and \( T_{r2} \) are turned-on, and the voltage \( w_{p1} \) equals \( E \) at the moment \( t_0 \), but the maximum value of the resonant current is given by the relation:

\[
I_{r} = (K' - 1)E' \sqrt{\frac{C_{n1} + C_{n2}}{L_r}} = K' - 1 \sqrt{\frac{C_{n1}}{L_r}} > I_r
\]
(4)

At the moment \( t_1 \), \( T_{r2} \) is turned-off while the capacitor \( C_{r1} \) continues to discharge until the voltage \( w_{p1} \) reaches zero, at the moment \( t_2 \). Between \( t_1 \) and \( t_2 \), the voltage \( w_{p1} \) is maintained zero due to the inverter diodes. Finally, at the moment \( t_3 \), the current \( i_t \) reaches a value \( I_2 \) lower than \( I_2 \).

In both cases shown in fig. 2a and b, it was considered that one switching of the inverter transistors takes place at the moment \( t_1 \).

Forward, the operating mode of the converter shown in fig. 1 is described during a switching process, for example, the one starting at the moment \( t_0 \) according to figs. 1 and 3.

At the moment \( t_0 \), the transistors \( T_{r1} \) and \( T_{r2} \) are on, the voltage on the primary winding of the RF transformer is equal to \( K'E' \) and the input inverter current \( i_t \) equals \( I_2 \).

At the moment \( t_1 \), the transistors \( T_{r1} \) and \( T_{r2} \) are turned-on, so between \( t_0 \) and \( t_2 \), the voltages \( w_{p1} \) and \( w_{p2} \) decrease from \((K' - 1)E' \) to zero and respectively, from \( K'E' \) to \( E' \) (figs. 2a and 2b).
Fig. 3

At the moment $t_1$, the current $i$ through the inductor $L_x$ reaches the value $(I_a-I')$. Then, only the capacitor $C_1$ continues to discharge through $T_{r1}$ until it reaches zero voltage at the moment $t_2$, since $T_{r2}$ is turned-off at the moment $t_1$. 

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The voltage \( v_1 \) remains zero up to the moment \( t_3 \), when the transistors \( T_1, T_2, T_3 \) are turned-off and the devices \( T_4 \) and \( T_5 \) are turned-on. Obviously, the moment \( t_3 \) is imposed by the converter command pattern.

At the moment \( t_3 \), the current \( i \) reaches a value \( id \) (fig. 3a).

Then, up to the moment \( t_4 \), capacitor \( C_{r1} \) charges from zero to the voltage \( v_{dc} \), through the diode \( D_{r1} \) and between \( t_4 \) and \( t_5 \), \( C_{r2} \) and \( C_{r3} \) overcharged  up to \( k' \) and respectively \( k + 1 \) \( E \). Between \( t_4 \) and \( t_5 \), the voltage \( v_2 - E \) is applied to the inverter's input. During the interval time, the current \( i \) becomes again equal to the inverter current \( id \). At the end of this interval time, a new operating cycle of DC/AC converter begins. On the constant operating regime of the converter the hatched areas in fig. 3a, which represent \( Q_1 \) - the electric charge lost by the capacitors and \( Q_2 \) - the electric charge received by the capacitors, become equal (thus \( Q_1 = Q_2 \)).

Finally, what follows, the waveforms of the output voltage \( v_2 \) on the terminals of the secondary winding of the transformer is explained, according to fig. 4.

Fig. 4
Fig. 4a shows the voltage \( v_t \) for two periods and fig. 4b shows the voltage \( v_z \) and the current \( i_z \). The \( \phi \) angle represents the phase difference between the fundamentals \( V_{1,0} \) and \( V_{2,0} \) of the two voltages. Along the two periods, the value of the load current \( i_z \) is considered as remaining constant. The switchings of the transistors \( T_1 \) - \( T_{10} \) occur at \( \phi, \pi + \phi, 2\pi + \phi, 3\pi + \phi \) angles and so on, when the voltage \( v_z \) is canceled.

Simultaneously with these switchings, the transistor \( T_E \) is turned-on at ZCS. After performing these switchings, the difference current \( (i_z - i_t) \) charges the switching capacitor \( C_t \) up to the voltage \( E \). The diode bridge opens and the excess of inductive energy flows into the capacitor \( C_t \) through the transistor \( T_E \). The necessary switching angle for the current \( i_z \) to change direction is \( \beta \) and it is shown in fig. 4b.

Its value is chosen so that \( \text{dv} / \text{dt} \) of the voltage on the secondary winding should be acceptable for the semiconductor devices. At the end of the switching angle \( \beta \), the ZVS of the transistor \( T_E \) takes place.

3. DC/AC Converter with one PWM Based Inverter

The operating principle of DC/AC converter with one PWM inverter and one RF intermediate circuit results from fig. 5a. By means of the cycloconverter having the \( T_1 \) - \( T_n \) transistors, on the load pulse trains are applied consisting of the integers \( p_1, p_2, ..., p_m \) of pulses.

These pulse trains are pulse width modulated according to a sinusoidal law so that the low order \( (n \sim 3, 5, 7, etc.) \) higher harmonics of the output voltage \( v_c \) of the cycloconverter have small values, generally less than 5% of the value of the fundamental amplitude \( V_{n,n} \).

For an output frequency \( f = 50 \text{Hz} \) of the fundamental voltage \( v_c(t) = V_0(1) \sin(2\pi ft) \) the pulse frequency \( f_p \) is adopted as 24 KHz. Since the voltage \( E \) of the accumulator battery can decrease with about 20% from its maximum value \( E_{\text{max}} \), in order to keep the fundamental amplitude \( V_{n,n} \) practically unchanged, certain modes of operation (for example A, B, ..., E) are chosen, differing from each other by the number of pulses obtained at the cycloconverter output.
For instance, fig. 5b shows the fact that within the interval \( \pi/12 \) and \( 2\pi/12 \), the pulse number can change between \( p_2 = 6 \) (for \( E_{\text{max}} \)) and \( p_2 = 8 \) (for 0.8 \( E_{\text{max}} \)).

At the same time, fig. 5c presents the variation of the pulse number \( p_2 \) within the interval \( 2\pi/12 \) and \( 3\pi/12 \).

The values of the pulse numbers on different intervals of the fundamental period are given in Table 1 depending on the chosen operation mode:

<table>
<thead>
<tr>
<th>OPERATION MODE</th>
<th>PULSE NUMBER</th>
<th>VOLTAGE E</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>p_1 8 p_2 12 p_3 16 p_4 19 p_5 20</td>
<td>80.19% ( E_{\text{max}} )</td>
</tr>
<tr>
<td>B</td>
<td>p_1 8 p_2 12 p_3 15 p_4 18 p_5 19</td>
<td>86.16% ( E_{\text{max}} )</td>
</tr>
<tr>
<td>C</td>
<td>p_1 7 p_2 11 p_3 15 p_4 17 p_5 18</td>
<td>90.81% ( E_{\text{max}} )</td>
</tr>
<tr>
<td>D</td>
<td>p_1 7 p_2 11 p_3 14 p_4 16 p_5 17</td>
<td>95.61% ( E_{\text{max}} )</td>
</tr>
<tr>
<td>E</td>
<td>p_1 6 p_2 10 p_3 13 p_4 15 p_5 16</td>
<td>100% ( E_{\text{max}} )</td>
</tr>
</tbody>
</table>

During the pauses when the voltage \( v_c \) vanishes (Fig. 5a), the current \( i_c \) closes through the transistors \( T_a \) and \( T_b \) or \( T_b \) and \( T_c \). Obviously, for the sake of simplicity in the control diagram of the DC/AC converter, only two of the cycloconverter's transistors are in conduction during one pause.

The two groups of transistors are in conduction alternatively, during two joining pause intervals. Certainly, during the pause intervals the resonant circuit and the inverter are not working, the transistors \( T_a \), \( T_b \) and \( T_a \), \( T_b \) being turned off.

At the beginning of a pause interval, the secondary winding of the ferrite transformer is still connected only with the switching capacitor \( C \) whose voltage increases with the permitted slope \( \Delta V/\Delta t \) up to the value \( E \). Since the primary winding is connected to the capacitor \( C \) having a reduced voltage \( v_c \cdot E \) (Fig. 4a), part of the energy stored by \( C \) will be transferred to the capacitor \( C_t \) by means of the diodes \( D_t - D_t \) and \( D_t \).

This energy transfer results in the increase of the DC/AC converter efficiency.

The higher harmonics in the spectrum of the output voltage \( v_c \) are those of the order \( (f_c, f_c /2 - 1) \) and \( (f_c, f_c /2 + 1) \). These harmonics can be considerably decreased by introducing the passive filter \( L_c - C_e \) at the cycloconverter output.

In fig. 6 are presented the ratios between the amplitudes \( V_{\text{out}} \) of the main higher harmonics of the voltage applied across the load, and the amplitude \( V_{\text{th}} \) of the fundamental corresponding to the A operation mode. One can draw the conclusion that, regarding the higher harmonics of the current passing through the load, their amplitude are smaller than 5%.

As the conclusion, the DC/AC converter proposed in fig. 1 is adequate for its application at relatively small output ranging between hundreds of W and some KW, only one ferrite transformer being enough in this case. What concerns the load impedance, its inductive power factor must be smaller than 0.9.

Certainly, in the case of an output frequency \( f_c = 60 \) Hz, other operation modes can be conceived, characterized by different pulses numbers.
4. DC/AC Converter with More Inverters with Asymmetric Control

Figure 7 presents the basic diagram of the DC/AC converter with an input resonant circuit, three inverters, three ferrite transformers and one cycloconverter having the I - I - I transistors.
The operating principle of this DC/AC converter results from fig. 8.
Here the signals $S_1$, $S_2$ and $S_3$ show the working durations of the three inverters with asymmetric control.

The waveforms of the voltages $v_1$, $v_2$ and $v_3$ applied at the primary windings of the ferrite transformers are identical with those presented in fig.4.

The voltage pulses obtained at the transformers output windings are summed and the means of the $T_1 - T_6$ transistors of the cycloconverter, the load voltage $v_L$ presented in fig.3, is obtained. The pulse frequency $f_p$ can be chosen 18 KHz (for $f = 50$ Hz) or 21.6 KHz (for $f = 60$ Hz).

These values were obtained considering that 360 pulses correspond to one fundamental period.

For this DC/AC converter more operation modes (A, B, C, ..., F) are also established, so that, when the voltage of the accumulator battery changes between 82.2% and 100% from the value $E_{max}$, the output voltage applied across the load remains practically unchanged.

These working modes can be obtained by eliminating, step by step, a number of pulses equal to $n = 2$ and $n = 5$, from the hachured surfaces in fig.8.

Table 2 presents, for a half-period, the limit values, given in grades, of the inverters working durations $S_1$, $S_2$ and $S_3$ for different working modes (A, B, C, ..., F).

<table>
<thead>
<tr>
<th>Working mode</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>Voltage $E$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>10° - 134°</td>
<td>26° - 154°</td>
<td>46° - 170°</td>
<td>82,20% $E_{max}$</td>
</tr>
<tr>
<td>B</td>
<td>10° - 129°</td>
<td>28° - 152°</td>
<td>51° - 170°</td>
<td>86,13% $E_{max}$</td>
</tr>
<tr>
<td>C</td>
<td>10° - 124°</td>
<td>30° - 150°</td>
<td>56° - 170°</td>
<td>89,89% $E_{max}$</td>
</tr>
<tr>
<td>D</td>
<td>10° - 119°</td>
<td>32° - 148°</td>
<td>61° - 170°</td>
<td>93,47% $E_{max}$</td>
</tr>
<tr>
<td>E</td>
<td>10° - 114°</td>
<td>34° - 146°</td>
<td>66° - 170°</td>
<td>96,85% $E_{max}$</td>
</tr>
<tr>
<td>F</td>
<td>10° - 109°</td>
<td>36° - 144°</td>
<td>71° - 170°</td>
<td>100% $E_{max}$</td>
</tr>
</tbody>
</table>

Figure 9 presents the ratios between the amplitudes $V_{n}$ of the most important higher harmonics of the voltage across the load, and the fundamental amplitude $V_{h}$ corresponding to the A operation mode.

A comparison between the higher harmonics spectrums related to the output voltages $v_1$ of the DC/AC converters according to figs. 6 and 9, reveals that the version presented in fig.7 is more advantageous, being characterized by a lower content of higher harmonics.

In the case of the DC/AC converter with three ferrite transformers, the higher harmonics of the current passing through the load can have amplitudes lower than 5% of the current fundamental value, under the condition that the load power factor is inductive and smaller than 0.95.

No doubt, DC/AC converters with more than three ferrite transformers can be conceived, and in this case the voltage higher harmonics will reduce even more.
As a conclusion, the DC/AC converter proposed in fig. 7 is adequate to be used for relatively high output powers, ranging between some KW and tens of KW.
Based on the diagrams presented in figs. 1 and 7, DC/AC converters can be realised whose output voltage in three-phased [9].

References:


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